The WB4VVF Accu-Keyer

BY JAMES M. GARRETT,* WB4VVF

IT IS QUITE POSSIBLE to send perfect code with a straight key. It has been pointed out to me, however, that my code left something to be desired. Also, because I have never quite grasped the fine art of holding a key firmly, I am Q5 at several hundred feet – audibly. Therefore, a keyer was deemed a necessity.

The price of commercial keyers is, however, quite high, if the keyer will do a reasonable amount of work – a requirement, since I am basically lazy. The Accu-Keyer is a result of trying to design the maximum keyer for the least cash outlay.

The Accu-Keyer has these features:

1) Self-completing dots and dashes
2) Dot and dash memories
3) Iambic operation
4) Dot and dash insertion
5) Automatic character space
6) 5-50 wpm speed range
7) Low cost

A synchronized clock provides uniform starting for constant-width characters. Also the dot-dash decision is made at the end of the space following the bit, allowing maximum leeway in paddle operation. The seven ICs used in the circuit can be purchased for three dollars or so total, while all the rest of the parts should come to less than twelve dollars including the printed circuit board, depending upon how good a scrounger you are. Total cost should be less than fifteen dollars, offering lots of performance for the money!

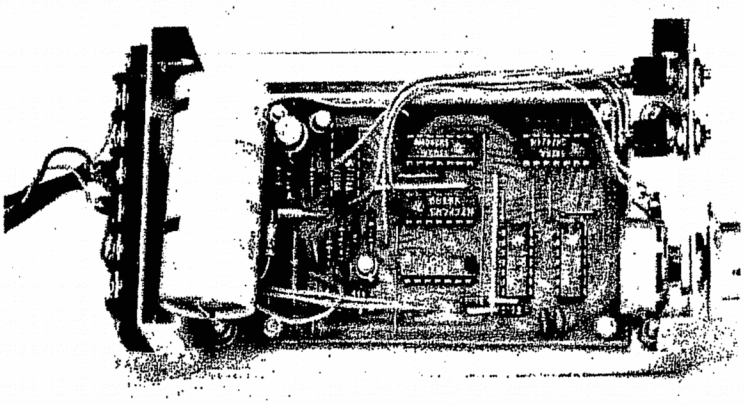
* 126 W. Buchanon, Orlando, FL 32809.

Logic Description

Three types of gates are used in the logic section of the keyer. There are three 7474 edge-triggered type *D* flip-flops, three 7400 quad two-input NAND gates, and one 7410 triple three-input NAND gate, for a total of seven dual-in-line packages. All the gates are TTL types.

The 7474 is a clocked edge-triggered type *D* flip-flop which has two modes of operation, synchronous and nonsynchronous. Nonsynchronous inputs are the SET (pin 1) and the RESET (pin 4) connections. These inputs can be used to force the Q and $\overline{Q}$ outputs into either a high or low condition. SET, when grounded, forces the Q output high and RESET, when grounded, forces the Q output low. The $\overline{Q}$ output is always in an opposite state from the Q output.

A synchronous input is provided (pin 2). If both the SET and RESET inputs are high and the clock pulse (pin 3) goes positive, the state of the *D* input (pin 2) will be transferred to the Q output, i.e., if *D* was high, Q will go high. This transition can occur only on the positive-going edge of the clock pulse.



The author's version of the Accu-Keyer is built into a Minibox. The keyer is powered from the 6.3-V ac line of the receiver filament supply. The rectifier and filter components are shown at the extreme left in this view.

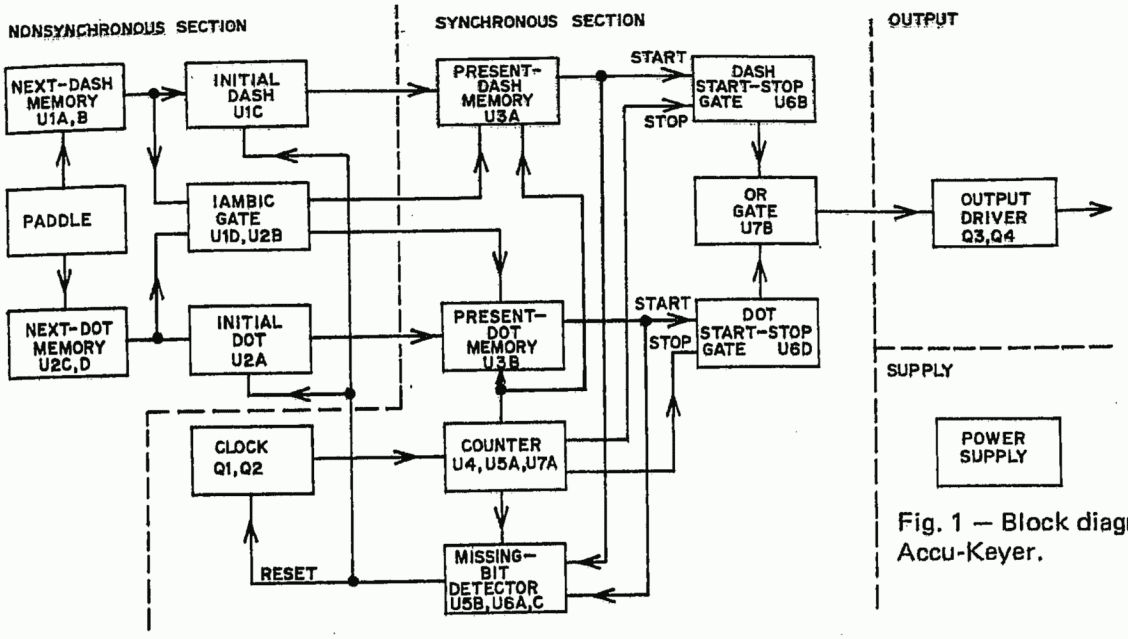


Fig. 1 — Block diagram of the Accu-Keyer.

The two- and three-input gates are NAND-type gates. Outputs of these gates are low only if all the inputs to the gates are high.

Block Diagram

Fig. 1 shows that the keyer is composed of four sections. In the nonsynchronous section the gates change logic state when the paddle is moved, while in the synchronous section the logic changes in step with the clock signal. The output driver changes the logic levels into voltages that will key the transmitter. The +5 volts is developed in the Zener-diode-regulated power supply.

The flip-flops and gates that perform the functions in the circuit are shown in the blocks. In the discussion that follows, a bit is defined as a single dot or dash and the space following.

The present-bit memories store the information as to which bit is being sent. These memories start the bit by enabling the start-stop gates. These outputs are fed through an OR gate to the output driver. A counter is also enabled at the start of a bit and disables the output at the beginning of the bit space.

Next-bit memories allow the keyer to remember one bit ahead. At the end of each bit four conditions are possible with the next-bit memories.

1) If the dot memory is on, the keyer will start a dot.

2) If the dash memory is on, the keyer will start a dash.

3) If both are on, the keyer will produce the opposite bit from the one it is sending.

4) If neither is on, the keyer will assume a missing bit and automatically give two additional spaces.

The iambic gate is used to produce the correct input to the present-bit memories for condition 3 above. At the end of condition 4, the missing-bit detector resets the clock and enables the initial dash-dot gates. These gates are used to start the keyer and synchronize the clock with the first bit sent.

Circuit Description

The following circuit description is included for those who like to "chase through the logic." In the discussion, the part designation is followed by a dash and the pin number of the logic package. Reference is made to the parts in the circuit diagram, Fig. 2. A timing chart for the synchronous portion of the keyer is plotted in Fig. 3. The sending of characters AB is shown.

Clock pulses for the keyer are generated by a relaxation oscillator consisting of Q1 and Q2 with associated parts. The base of Q1 is biased at about 1.4 volts by R1 and R2. R4 and R7, in series with the output resistor, R6, connect the emitter to ground. This combination is bypassed by the timing capacitor, C1. Q1 will therefore be biased on and some current will flow through the collector resistor, R3, producing a voltage drop which will start to turn on Q2, a pnp device. The Q2 collector will start going positive, forcing Q1 to turn on harder through the speed-up capacitor, C2. C1 will be forced to charge because of the current gain of Q1. At some positive voltage, Q1 will saturate and the charge across C2 will no longer be sufficient to supply base current to the transistor. Therefore, Q1 will turn off, causing Q2 to turn off and the output will return to zero. The emitter-base junction of Q1 will be reverse biased until C1 in the emitter circuit discharges through R4, R6, and the speed control, R7. A short positive-going pulse with a varying period, depending on the speed control setting, is produced across R6 as a result of this action.

A reset input is provided by CR1 to allow the clock to start in synchronism with the paddle. This input holds the emitter of Q1 at a high level and prevents the clock from oscillating when no code is being sent.

Synchronous Operation

Referring to the timing diagram, Fig. 3, t1 is the time the keyer paddle is closed for a dot. Logic levels are shown for the points prior to this time.

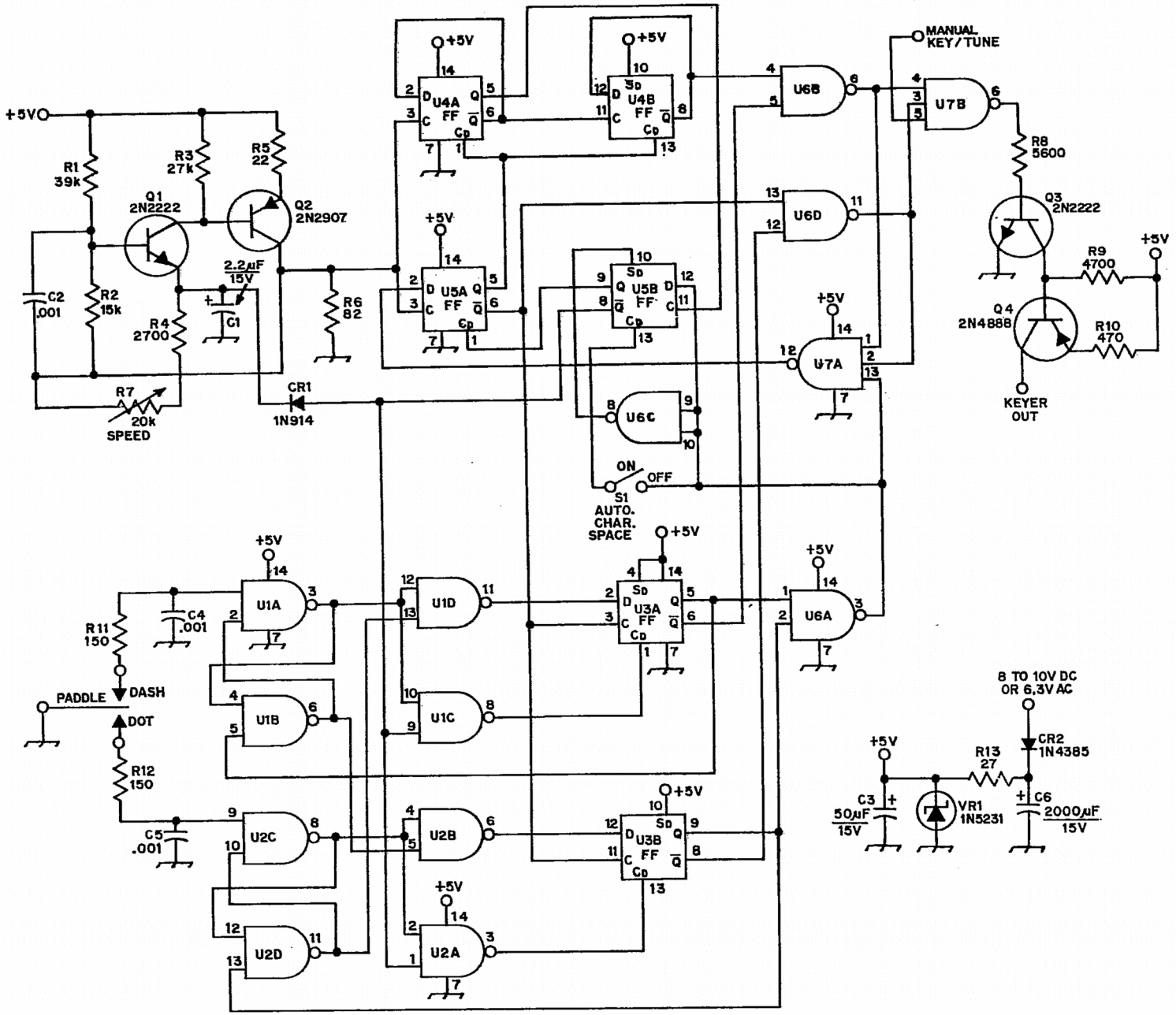


Fig. 2 — Schematic diagram of the Accu-Keyer. Resistances are in ohms; k = 1000. All capacitances are in microfarads. All resistors may be 1/4 watt except R13, which should have a 2-W rating. Capacitors with polarity indicated are electrolytic; all others are disk ceramic. Parts not listed below are for text reference and circuit-board identification.

CR1 — Small-signal silicon diode.

CR2 — Rectifier diode, 1/2 A or greater.

Q1, Q3 — Silicon npn, 250-mW, high-speed switching or rf-amplifier transistor.

Q2 — Silicon pnp, 250-mW, high-speed switching or rf-amplifier transistor.

Q4 — Silicon pnp, 250-mW, high-voltage af-amplifier transistor.

R7 — Reverse-log-taper control; Mallory U-28 suitable.

S1 — Spst toggle.

U1, U2, U6 — Quad 2-input NAND gate, type 7400.*

U3, U4, U5 — Dual type *D* flip-flop, type 7474.*

U7 — Triple 3-input NAND gate, type 7410.*

VR1 — 5.1-V, 0.5-W Zener diode.

* All ICs are dual-in-line package, 14 pin. Note: All ICs are available from various manufacturers or as surplus. Motorola part numbers are prefixed by *MC* and suffixed by *P*. Texas Instruments parts have an *SN* prefix and *N* suffix. Signetics ICs have an *N* prefix and an *A* suffix. For example, Motorola's MC7400P is equivalent to Texas Instruments' SN7400N or Signetics' N7400A.

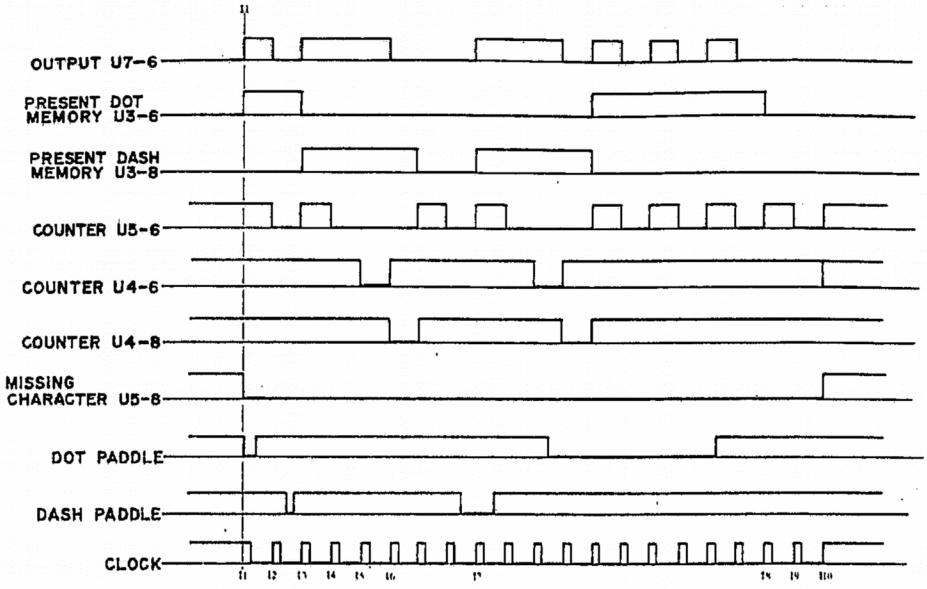


Fig. 3 — Timing diagram for the Accu-Keyer.

The upper plot is U7-6, which is the output of the keyer. At t1 the dot paddle is closed, producing a ground on U3-13, as will be explained later. This forces U3-8 high, U3-9 low, U6-3 high, and U6-8 low, causing U5-9 to go high and U5-8 to go low. The reset to the clock is removed, allowing the clock to produce a pulse at t2. Prior to the paddle closure, U5-9 was low, forcing U5-5 low. The U5-5 low caused U4-6 and U4-8 to be high. Therefore at t1, U6-12 will have a high from U3-8 and U6-13 will have a high from U5-6. U6-11 will be low causing U7-6 to go high, starting the dot and producing a high on U7-12.

At t2 the clock pulse occurs on U4-3 and U5-3. Because U4-6 is being held high by U5-5 low, it will not change state. The reset on U5-1 has been removed at t1. Because U5-2 is high, U5-5 will be clocked high and U5-6 low. The output at U7-6 will then go low because of the low on U6-13 stopping the dot. U7-12 will again go low.

At t3, either pin 2 or 12 of U3 will be low, as explained later, depending on which bit is required next. In this example pin 2 is low calling for a dash. At t3 the clock once again pulses and U5-6 will go positive because U5-2 is low. U3-3 will get a positive-going clock pulse and therefore U3-6 will go high and U3-5 low. U5-10 will always be held low by either a low on U6-1 or U6-2, as long as a character is being sent, because either U3-5 or U3-9 will be low. Therefore the clock will continue to run. A high on U3-6 will mean a high at U6-5, and because U6-4 is high the output at U7-6 will go high. Once again U5-2 will be high.

At t4, U5-6 will go low and U5-5 high, removing the resets from U4-1 and U4-13. At t5, U5-3 is clocked, but since the output on U5-5 is high and U5-2 is still high, nothing happens. U4-6 goes low, however, because of the high on U4-2. Because U4-6 is tied to U4-2, it will continue to change state at each clock pulse, as the input state is never the same as the output. Therefore at t6, U4-6 will go high, clocking U4-11 and causing U4-8 to go low cutting off the output and placing U5-2 low again.

Automatic Character Generation

If U5-6 goes high and neither of the U3 inputs are low, such as at t8, the reset is removed from U5-10. At t9, U5-6 goes low removing the reset from U4-1. Therefore at t10, U4-5 goes high clocking U5-11 and causing U5-9 to go low, resetting U5-5 low and U5-6 high. This provides another positive clock at U3 and if no bit has been called for the clock is held and the keyer waits for another low on U3-1 or U3-13. If either U3-2 or U3-12 were low, as at t7, the keyer continues and generates another bit. The AUTO CHARACTER SPACE switch, S1, shorts U5-13 and U5-12 causing the clock to be reset immediately on detecting a missing bit at U6-3.

Asynchronous Circuitry

The purpose of this circuit is to provide an input to U3 commanding a bit at the end of the space of the last bit. As seen previously, this occurs when the present-bit memories are clocked. The circuit consists of six NAND gates cross coupled to form set-reset flip-flops and two gates to allow the keyer to start after the clock has been reset. The dot and dash sections are both the same so only one will be explained.

When the clock is reset, U3-5 and U3-9 will be high. Grounding one of the paddles, the dash paddle in this example, will force U1-3 high, and since both U1-4 and U1-5 are high, U1-6 will go low causing U1-3 to remain high. The paddle just needs to be tapped, therefore. U1-9 is high because the clock-reset line is high, so U1-8 will go low starting the synchronous operation described earlier. Henceforth, both the U1C and U2A sections are disabled by the low reset signal.

The output of U3-5 will go low during the time of the bit as can be seen by the timing diagram. At the end of this interval U3-2 will be clocked. If the paddle is released before then, the flip-flop consisting of U1A and U1B will be reset because of the low fed to U1-5 from U3-5. Assuming the input from the dot circuit U1-13 to be high, U3-2 will go

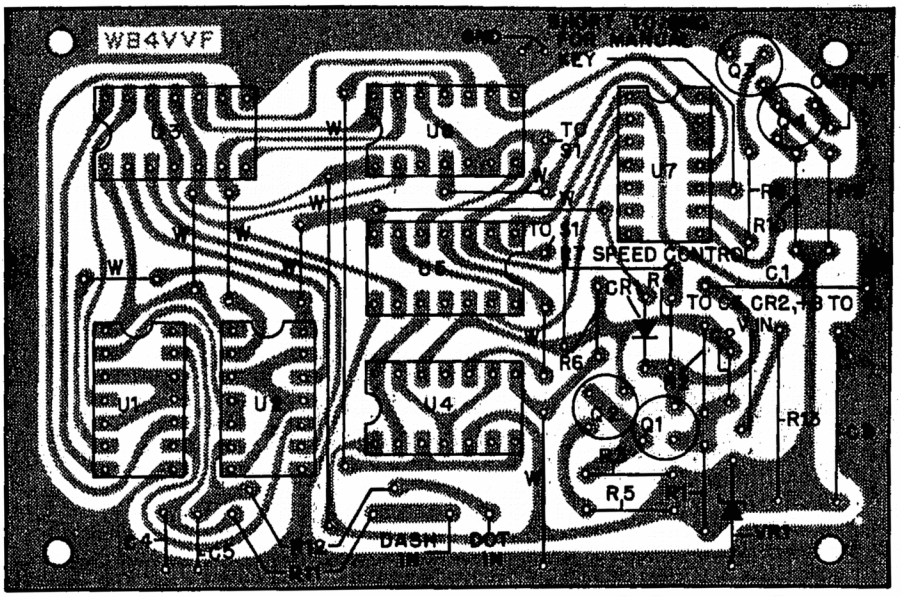


Fig. 4 — Etching pattern and parts-layout diagram for the Accu-Keyer. Pattern is actual size, shown from *foil side* of board. Ready-made circuit boards are available through the author.

high when the paddle is released. This prevents generating a double dot with a single tap of the paddle. The paddle contacts must therefore be held closed to generate consecutive dots or dashes.

If both paddles are held or if one of the paddles is tapped during a bit opposite to the one being sent, iambic operation calls for the next bit to be opposite. This provides for dot and dash insertion. When both paddles are held, both U1-3 and U2-8 are high. Therefore, both U3-2 and U3-12 would be low if it were not for the iambic gates U1D and U2A. Assuming that a dash is being sent, U1-6 will be low, causing a high on U2-5 and therefore a low on U3-12. However, U2-11 and U2-13 will be low, thus forcing U3-2 high. The inputs will continue to reverse as long as both paddles are held, thereby generating alternate dots and dashes.

Output Driver

The output from U7-6 is applied to Q3, which in turn drives Q4. Q3 is driven into saturation causing the base of Q4 to approach chassis-ground potential. The current through Q4 is determined by R10 and is set to about 10 mA. Q4 will withstand −100 volts when turned off. This should be adequate for most modern transmitters.[1] Obviously this keyer is designed only to drive transmitters using negative grid-block keying. If cathode keying is desired, an additional transistor may be used to key the cathodes directly or through a relay.

Power Supply

The 5 volts is regulated by R13, VR1, and C3. CR2 is used if operation from 6.3 volts ac is required. The current through R13 should be 100 mA for proper regulation.

[1] [EDITOR'S NOTE: Some grid-block-keyed transmitters may develop more than 100 volts across the keying terminals under key-up conditions. If this is the case, a fixed-value resistor may usually be shunted across the key line to lower the voltage somewhat. The resistance value should be high enough to prevent keying of the transmitter, usually a few hundred thousand ohms to a few megohms.]

Construction

A printed-circuit card has been laid out for the keyer containing all parts except the controls, filter capacitor, and rectifier in the power supply. The board will fit neatly in a 3 × 2 × 5-inch Minibox as shown in the photograph. A terminal strip is mounted along the rear to handle the inputs and outputs. There is ample room to mount a small 6.3-volt power transformer if operation from 117-V ac is desired. At my station the keyer is powered by the filament supply in the receiver.

Fig. 4 is an actual-size board layout and parts-placement guide for those desiring to build their own boards. A ready-made board is available from the author at a cost of $3.50. This is a glass-epoxy, mil-grade predrilled board, so no profit is being made at this price. A stamped return envelope would sure be appreciated!

It is essential that all leads to the keyer be shielded from rf. I use RG-174/U coax, which is small and does not take up as much space as the audio type of shielded cable. A .01-μF bypass capacitor is provided on the power input to remove rf. As shown on the diagram, the inputs from the paddle are filtered by 150-ohm resistors bypassed by .001-μF capacitors. In stubborn cases it may be necessary to bypass the paddle contacts at the paddle itself.

Substitution of transistors for Q1 and Q2 may require changing the value of R5 to make the first clock pulse the same length as the rest. Both should be transistors with a beta of at least 60. Q3 is noncritical, and any good silicon transistor should work. Q4 should be capable of withstanding the transmitter key-up voltage. Any pnp silicon device having a reasonable beta and meeting this requirement should work. The value of C1 may be juggled to change the range of the speed control. The value specified gives a range of approximately 5 to 50 wpm.

I would like to thank Duke Contini, W4YUU, and Dave Phillips, WB4UOC, for their suggestions and comments on the evaluation of the keyer. QST